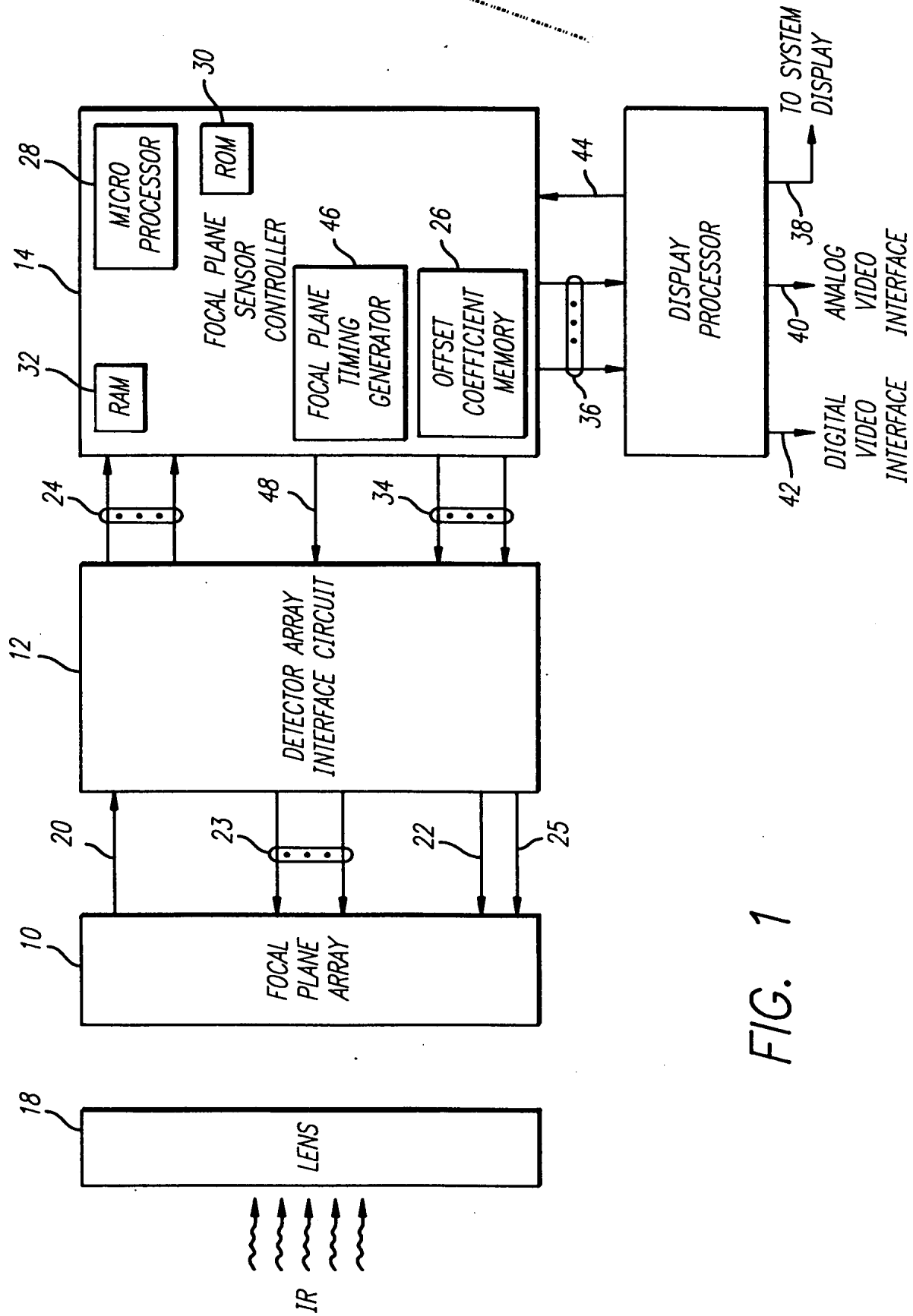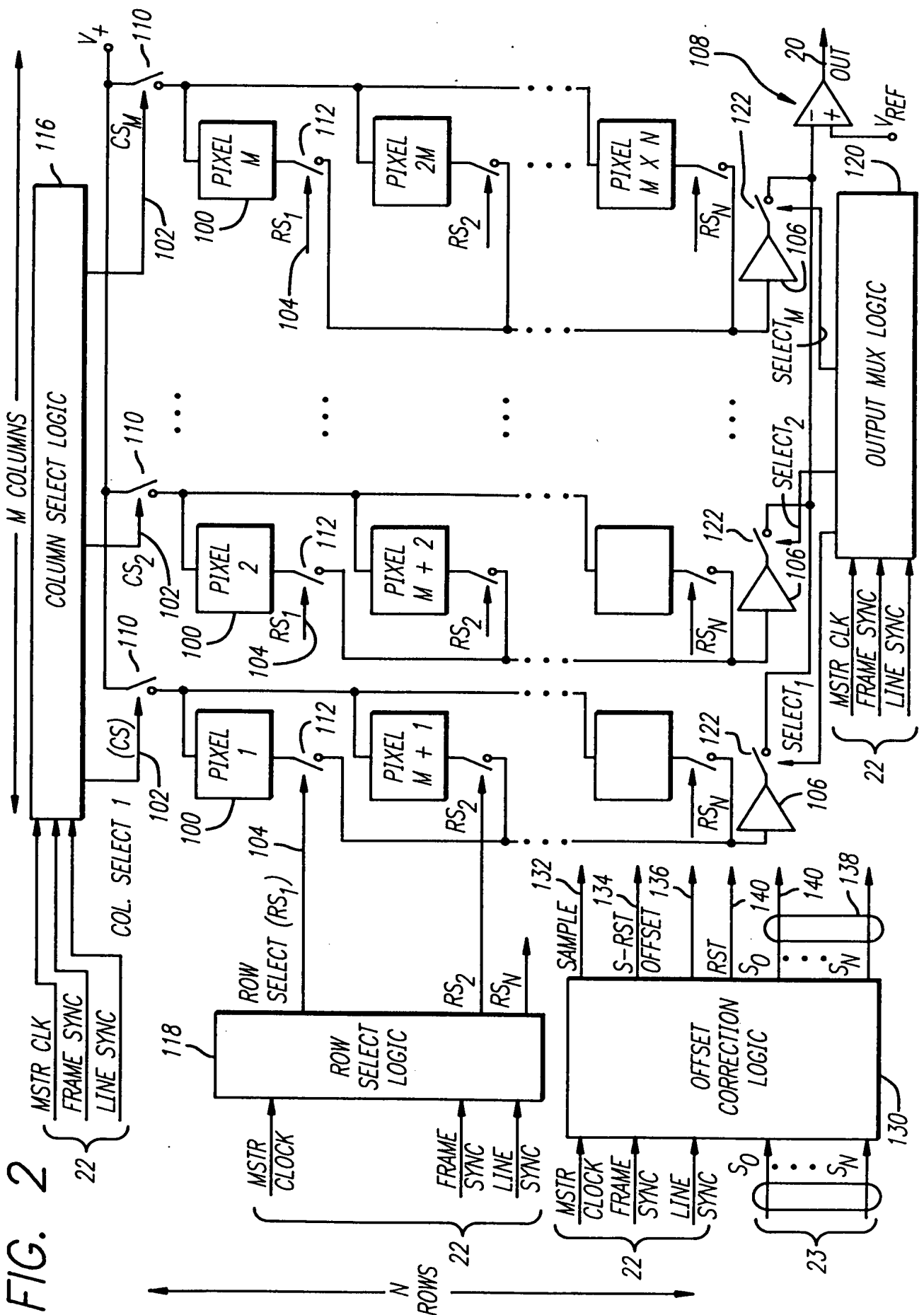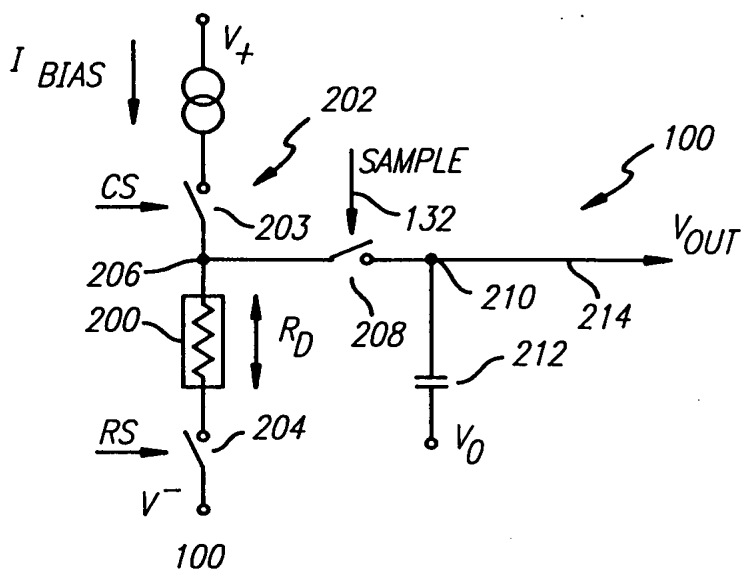5811808

FIG. 1

FIG. 2

FIG. 3A

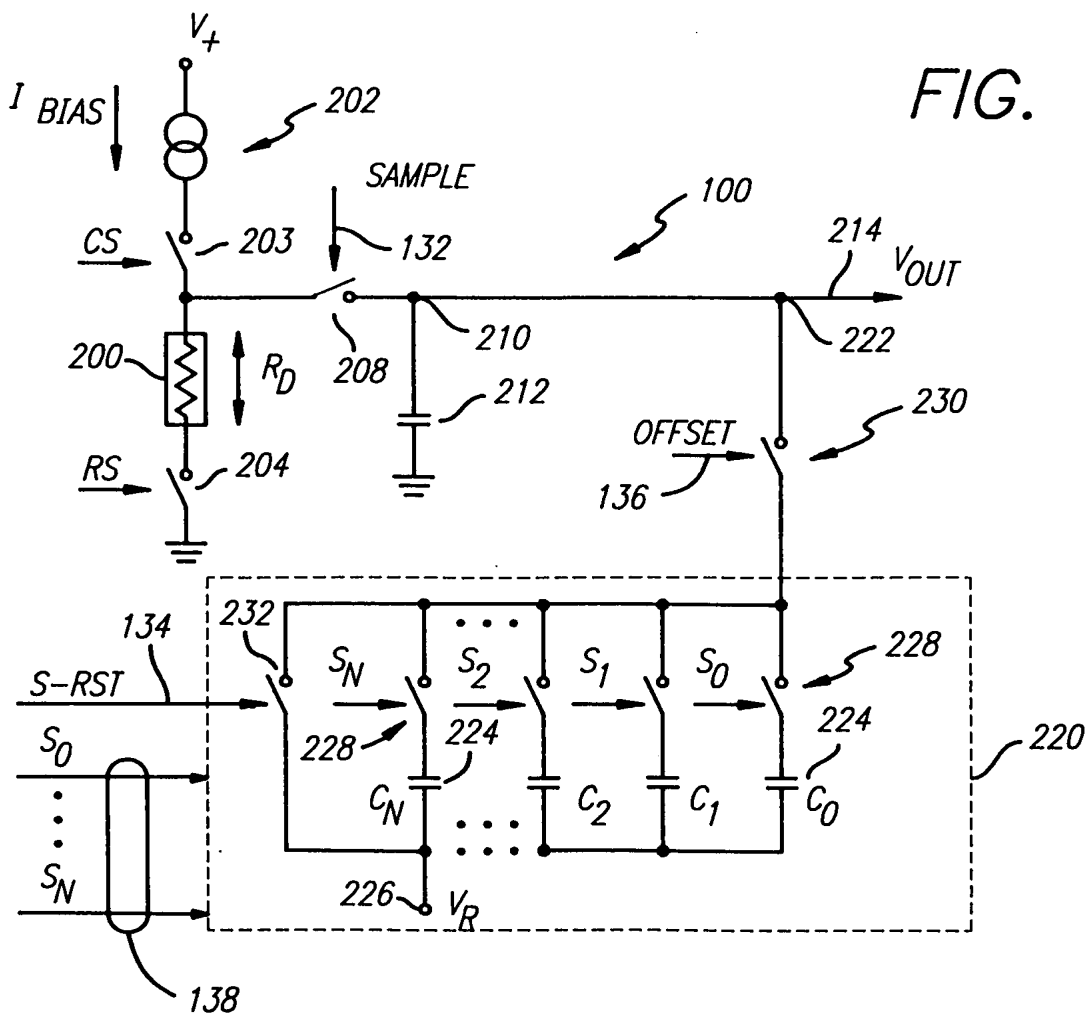

FIG. 3B

FIG. 3C
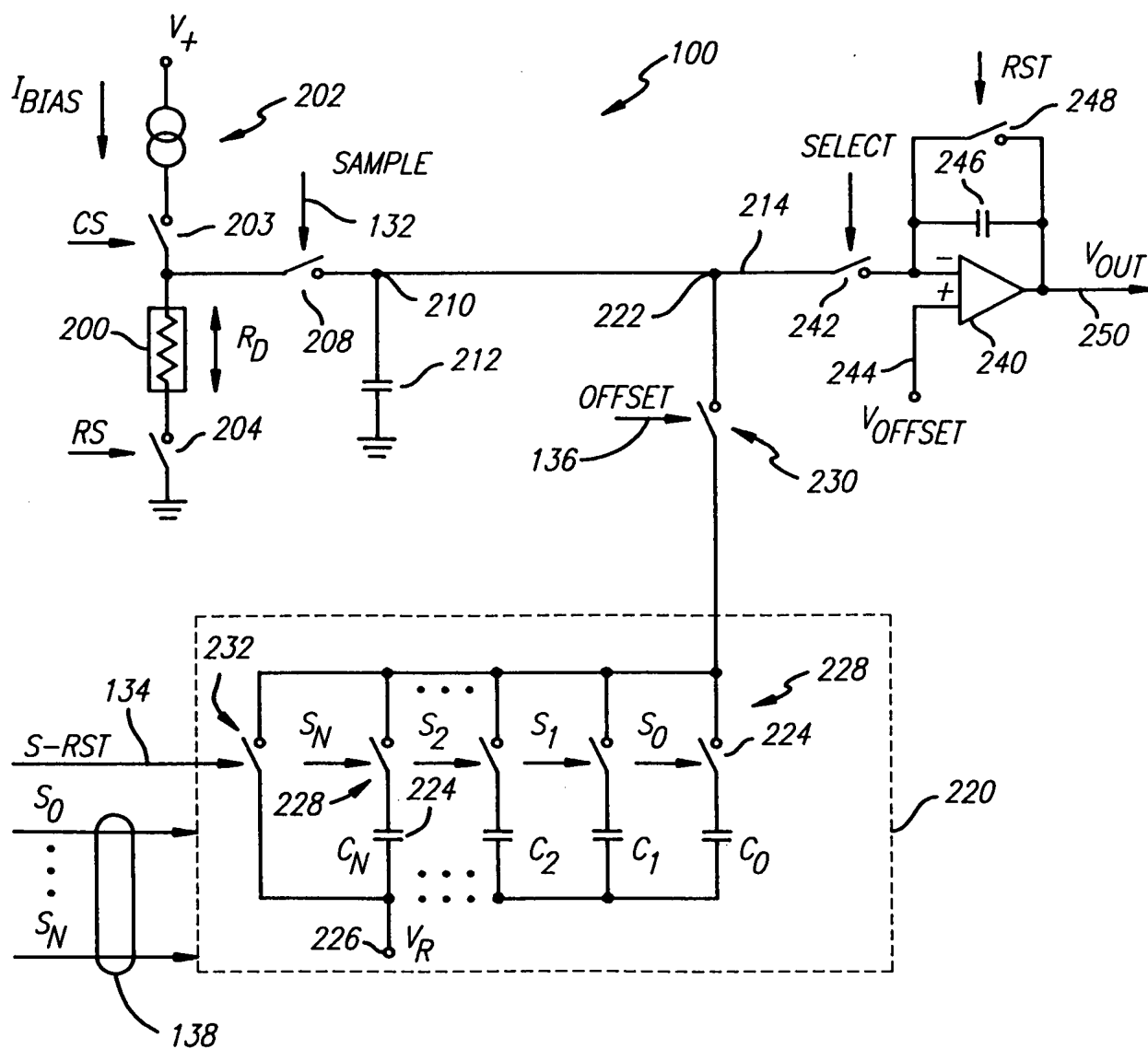
FIG. 4
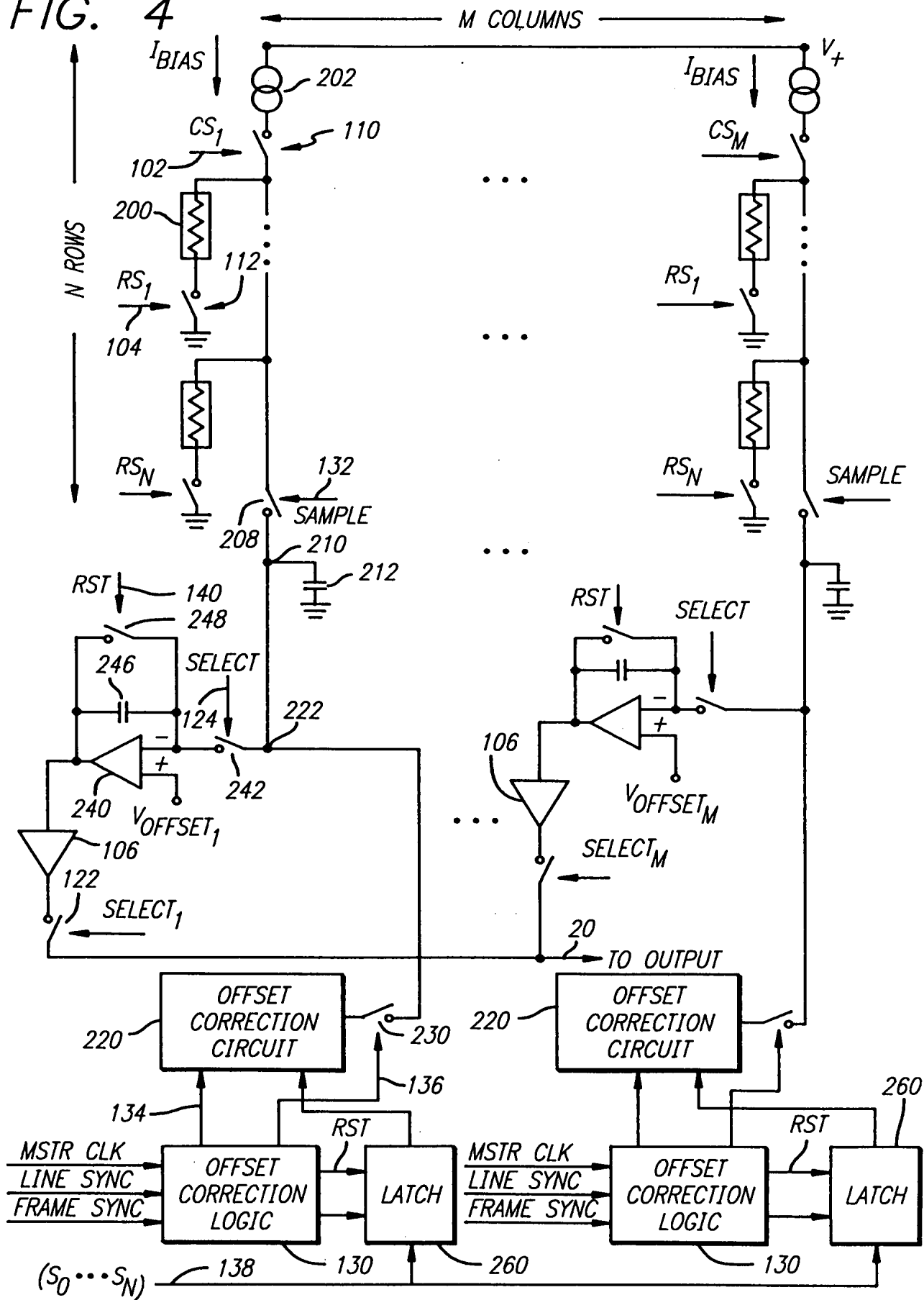
FIG. 5A
RS
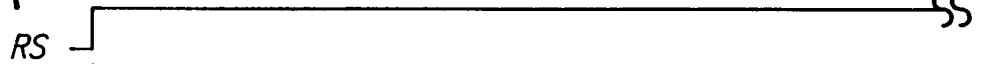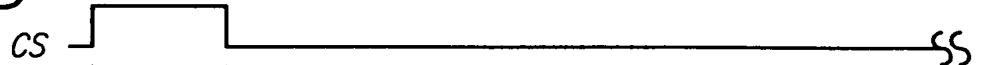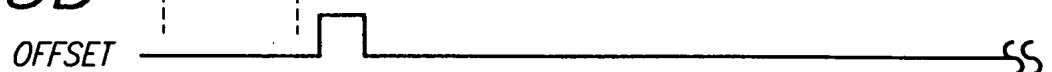
FIG. 5B
CS

FIG. 5C
SAMPLE

FIG. 5D
OFFSET

FIG. 5E
SELECT

FIG. 5F
S-RST

FIG. 5G
S_0

FIG. 5H
S_1

FIG. 5I
S_2

FIG. 5J
S_3

FIG. 5K
RST

FIG. 6A

SELECT
MSTR CLOCK

FIG. 6B

LINE SYNC

FIG. 6C

S0

FIG. 6D

S1

FIG. 6E

S2

FIG. 6F

S3
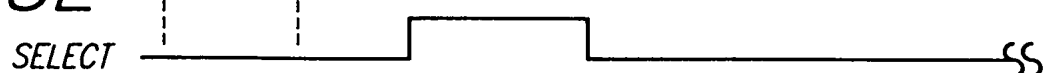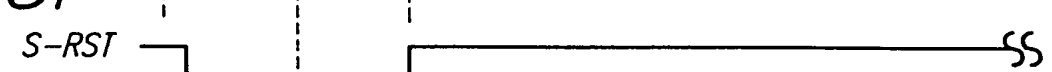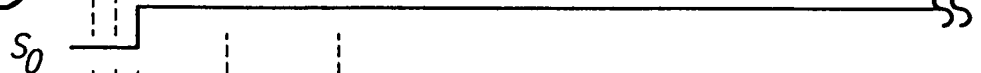
FIG. 6G

BINARY
OFFSET
COEFFICIENT

0011 1011 1111 0011 1010 1000 1000 1100 0100 1100
1011 1111 0011 0001 1010 0000 1100 0100 0100 1100

TIME →

FIG. 7

SAMPLED
VOLTAGE (V_D)

$P_{5,3}$ $P_{6,3}$ $P_{7,3}$ $P_{8,3}$ $P_{9,3}$ $P_{10,3}$ $P_{11,3}$ $P_{12,3}$ $P_{13,3}$ $P_{14,3}$

V_D'

TIME →

FIG. 8


```
┌────────────┬──────────────────────────────────┬──────────────┐
│  OUTPUT    │      COLUMN SELECT LOGIC         │    BIAS      │
│  DRIVER    ├──────────────────────────────────┤  CIRCUITS    │
│            │ OUTPUT AMPLIFIERS & OUTPUT MUX LOGIC │            │
```
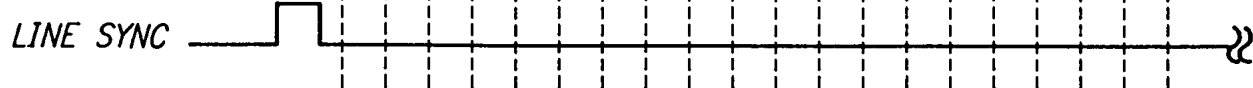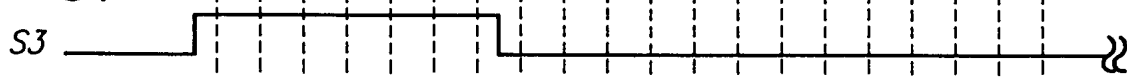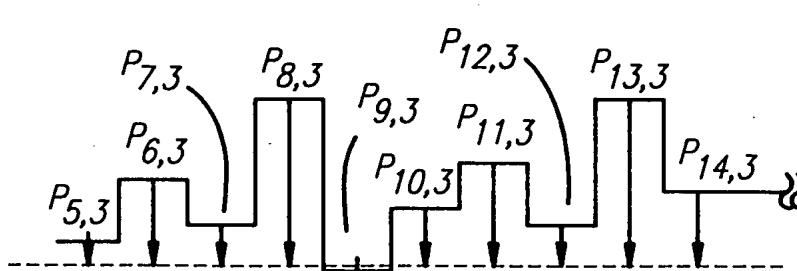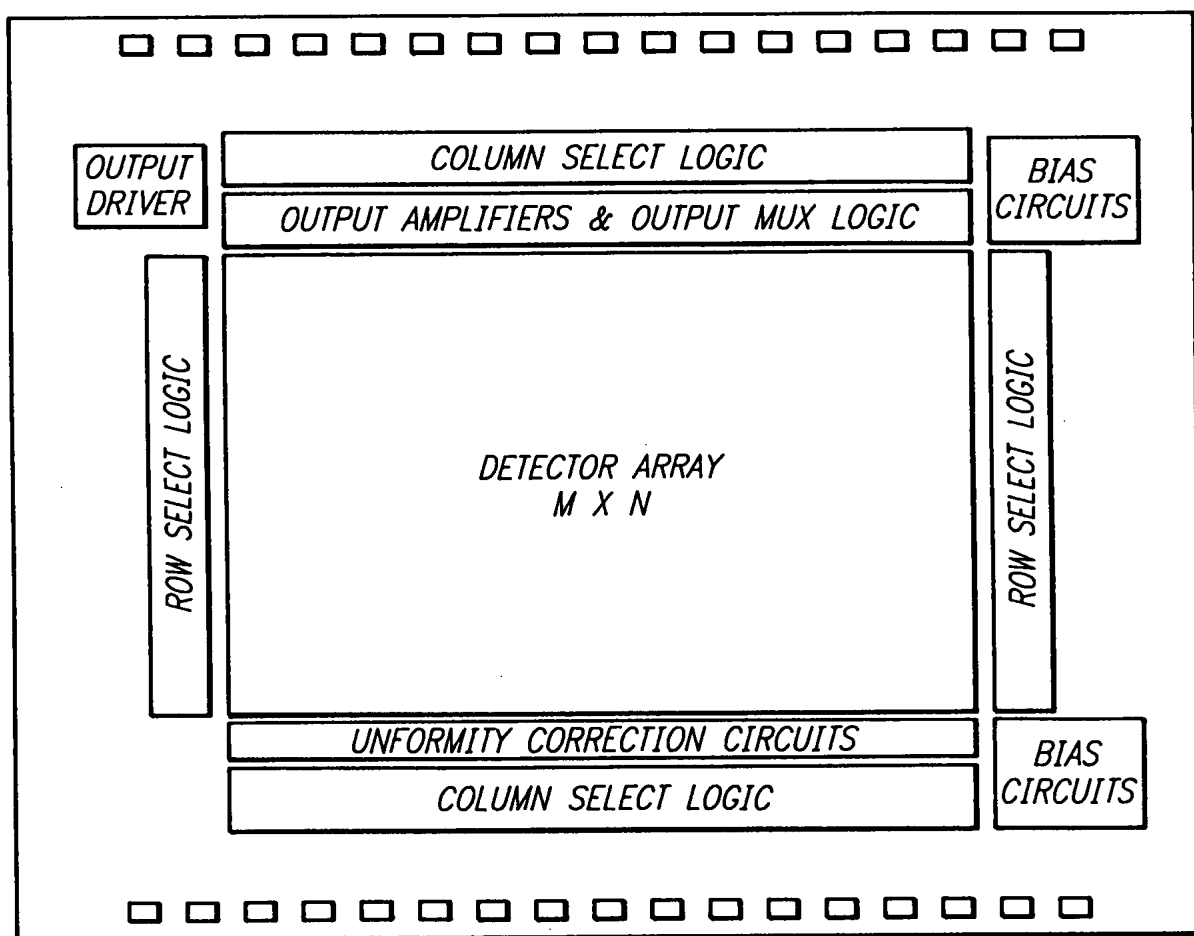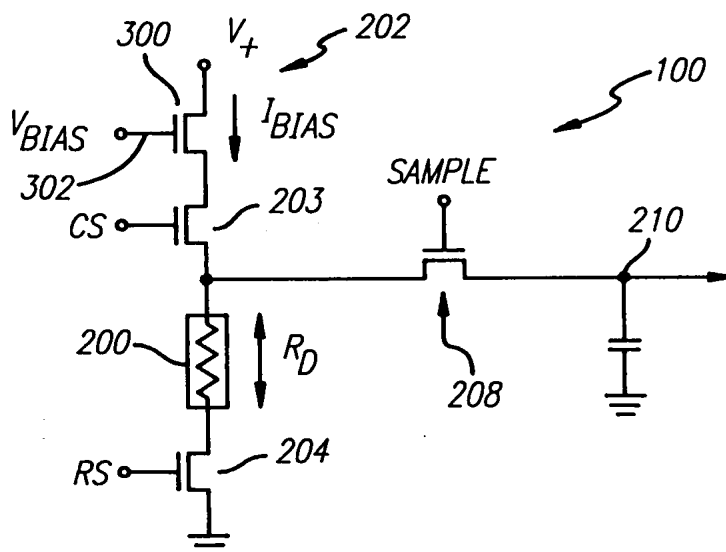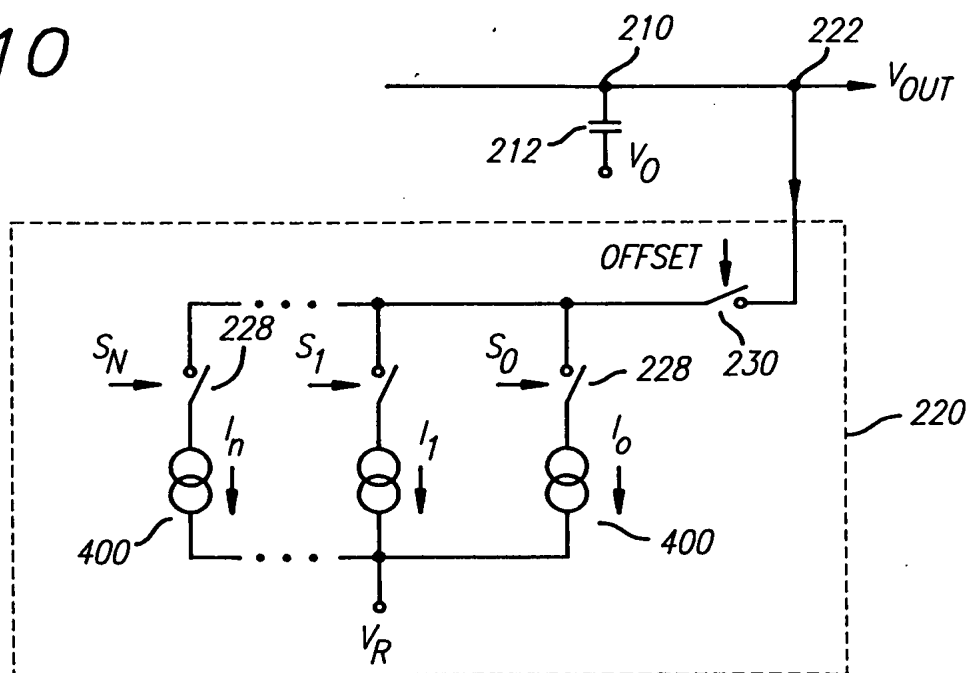
OUTPUT DRIVER

COLUMN SELECT LOGIC

OUTPUT AMPLIFIERS & OUTPUT MUX LOGIC

BIAS CIRCUITS

ROW SELECT LOGIC

DETECTOR ARRAY
M X N

ROW SELECT LOGIC

UNFORMITY CORRECTION CIRCUITS

COLUMN SELECT LOGIC

BIAS CIRCUITS

FIG. 9

V_+

300

V_{BIAS}

302

I_{BIAS}

202

100

CS — 203

$SAMPLE$

210

200 — R_D

208

RS — 204

FIG. 10

FIG. 11

FIG. 12